WHAT IS CLAIMED IS:

1. A capacitor having two nodes, comprising:
a first transistor coupled to one of the two nodes; and
a second transistor coupled to the first transistor and to a second one of the two nodes.

2. The capacitor of claim 1 wherein the first and second transistors each comprises a metal oxide semiconductor (MOS).

3. The capacitor of claim 2 wherein the first and second transistors each comprises a gate, the gate of the first transistor being coupled to the gate of the second transistor.

4. The capacitor of claim 3 further comprising a bias resistor coupled to the gates of the first and second transistors.

5. The capacitor of claim 2 wherein the first and second transistors each comprises a drain and source, the drain and the source of the first transistor being coupled to said one of the two nodes and the drain and source of the second transistor being coupled to said second one of the two nodes.

6. The capacitor of claim 2 wherein the first and second transistors each comprises a gate, drain and source, the gate of the first transistor being coupled to the gate of the second transistor, the drain and the source of the first transistor being coupled to said one of the two nodes, and the drain and source of the second transistor being coupled to said second one of the two nodes.

7. The capacitor of claim 6 further comprising a bias resistor coupled to the gates of the first and second transistors.

8. An integrated circuit comprising a capacitor having two nodes, a first transistor coupled to one of the two nodes, and a second transistor coupled to the first transistor and to a second one of the two nodes.

9. The integrated circuit of claim 8 wherein the first and second transistors each comprises a metal oxide semiconductor (MOS).

10. The integrated circuit of claim 9 wherein the first and second transistors each comprises a gate, the gate of the first transistor being coupled to the gate of the second transistor.

11. The integrated circuit of claim 10 wherein the capacitor further comprises a bias resistor coupled to the gates of the first and second transistors.

12. The integrated circuit of claim 9 wherein the first and second transistors each comprises a drain and source, the drain and the source of the first transistor being coupled to said one of the two nodes and the drain and source of the second transistor being coupled to said second one of the two nodes.

13. The integrated circuit of claim 9 wherein the first and second transistors each comprises a gate, drain and source, the gate of the first transistor being coupled to the gate of the second transistor, the drain and the source of the first transistor being coupled to said one of the two nodes, and the drain and source of the second transistor being coupled to said second one of the two nodes.

14. The integrated circuit of claim 13 wherein the capacitor further comprises a bias resistor coupled to the gates of the first and second transistors.

15. A tunable capacitor array, comprising:

a plurality of capacitors each having first and second nodes, a first transistor coupled to the first node, and a second transistor coupled to the second node, the first nodes of the capacitors being coupled together and the second nodes of the capacitors being coupled together; and

a plurality of switches each being positioned between a different one of the capacitors and the respective capacitors first or second node.

16. The tunable capacitor array of claim 15 wherein the first and second transistors for each of the capacitors each comprises a metal oxide semiconductor (MOS).

17. The tunable capacitor array of claim 16 wherein the first and second transistors for each of the capacitors each comprises a gate, the gate of the first transistor being coupled to the gate of its respective second transistor.

18. The tunable capacitor array of claim 17 wherein the capacitors each comprises a bias resistor coupled to the gates of the respective capacitors first and second transistors.

19. The tunable capacitor array of claim 16 wherein the first and second transistors for each of the capacitors each comprises a drain and source, the drain and the source of the first transistors being coupled to the first nodes, and the drain and source of the second transistors each being coupled to the second nodes.

20. The tunable capacitor array of claim 16 wherein the first and second transistors for each of the capacitors each comprises a gate, drain and source, the gate of the first transistor each being coupled to the gate of its respective second transistor, the drain and the source of the first transistors each being coupled to the first nodes, and the drain and source of the second transistors each being coupled to the second nodes.

21. The tunable capacitor array of claim 21 wherein the capacitors each comprises a bias resistor coupled to the gates of its respective first and second transistors.